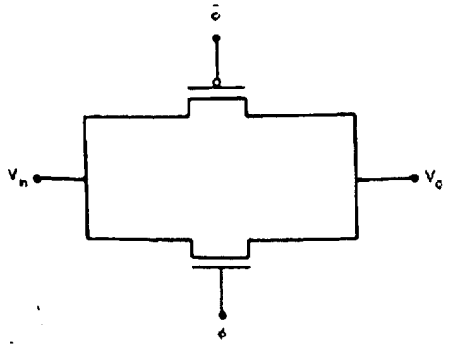
REMARKS

Applicant wishes to thank the Examiner for his examination of the present application. Previously withdrawn claims 21-28 have been cancelled. Claims 1, 5, 8, 15, 32 and 35 have been clarified by changing the term "complimentary switch" to "transmission gate." In the context of the subject patent application, and as known in the art of switching electronics, the term "complimentary switch" is interchangeable with "transmission gate." For support, see the subject application at Fig. 4 and page 10, line 28 to page 11, line 8; section 2.5 on page 55 of Weste, Neil and Eshraghian, Kamran, *Principles of CMOS VLSI Design*, Addison-Wesley, Reading, Massachusetts, 1985; and page 1-6 of Rung-Bin Lin, Chapter 1: Introduction to CMOS Circuits, http://vlsi.cse.yzu.edu.tw/education/vlsi_design/chapter1.pdf. No new matter has been added.

35 U.S.C. §103

Claims 1-3, 5-11, 13-15, 18, 20, 29, and 32-37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. patent number 6,538,491 (Spanoche) in view of U.S. patent 5,828,620 (Foss et al., hereinafter Foss). Amended claim 1 defines, in part, a multi-stage circuit that includes a bootstrap module. The bootstrap module includes a transmission gate.

Spanoche discloses a bootstrap circuit (see Spanoche at col. 13, lines 24-30). However, nowhere does Spanoche disclose that the bootstrap circuit includes a transmission gate. Foss discloses a charge pump circuit having a plurality of transistors (see Foss at Fig. 3), but the transistors are not configured to form a transmission gate. More particularly, as known by one of ordinary skill in the art (see for example, Weste, Neil and Eshraghian, Kamran, *Principles of CMOS VLSI Design*, Addison-Wesley, Reading, Massachusetts, 1985 at page 55, a copy of which is attached herewith), an exemplary transmission gate is shown below.



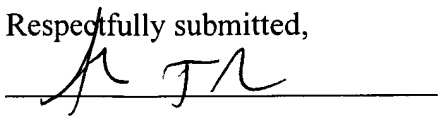
While the charge pump depicted in Fig. 3 of Foss includes both N-channel and P-channel transistors, clearly none of the transistors in Foss are configured to form a transmission gate.

Accordingly, since neither Spanoche nor Foss teach or suggest a bootstrap module that includes a transmission gate as required by claim 1 as amended, amended claim 1 is allowable over Spanoche and Foss. Dependent claims 2, 3, 5-7 and 29 are allowable for the same reason, and are further allowable in view of the additional limitations set forth therein. Independent claim 8 and dependent claims 9-11, 13, and 14 include a bootstrap module having a complementary switch and thus are also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein. Independent claim 15 and dependent claims 18 and 20 include a means for applying a bootstrap voltage that includes a transmission gate, and thus are also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein. Independent claim 32 and dependent claims 33-37 include a bootstrap module that includes a complimentary switch, and thus are also allowable for the same reasons as discussed above with regard to amended claim 1, and are further allowable in view of the additional limitations set forth therein.

Consideration of the application and issuance of a notice of allowance are respectfully requested. It is believed that a one month extension of time is required for this matter. Applicant hereby petitions for same and requests that any extension or other fee required for timely consideration of this application be charged to Deposit Account No. 19-4972.

If the Examiner has any questions as to the allowability of the currently pending claims or if there are any defects which need to be corrected, the Examiner is invited to speak to the Applicants' counsel at the telephone number given below.

Respectfully submitted,



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3/1. For an inverter with slightly lower noise immunity a β_n/β_p of 4/1 may be used which parallels the popular nMOS ratio rule [MeCo80]. This inverter finds use in circuits where an "n-rich" circuit is required and the power dissipation can be tolerated. Typical uses include static ROMs and PLAs. Note that the circuit could use n-load devices and p-active pull-ups, if this was of advantage.

Another inverter of interest is the tri-state inverter shown in Fig. 2.20. When CL = '0', the output of the inverter is in a tri-state condition (the Z output is not driven by the A input). When CL = '1', the output Z is equal to $\overline{A}$. For the same sized n- and p-devices, this inverter is approximately half the speed of the inverter shown in Fig. 2.10. This inverter will be discussed in more detail in Chapter 5, as it forms the basis for various types of clocked logic, latches, multiplexers, and I/O structures.

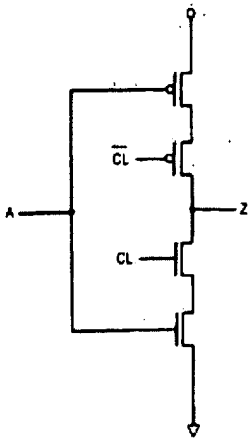

FIGURE 2.20. CMOS tri-state inverter

2.5 Transmission gate — DC characteristics

The transistor connection for a complementary switch or transmission gate is reviewed in Fig. 2.21. It consists of an n-channel transistor and a p-channel transistor with separate gate connections and common source and drain connections. The control signal ϕ is applied to the gate of the n-device, and its complement $\overline{\phi}$ is applied to the gate of the p-device. The operation of the transmission gate can be best explained by considering the characteristics of both the n-device and p-device as pass transistors individually. We will address this by treating the charging and discharging of a capacitor via a transmission gate.

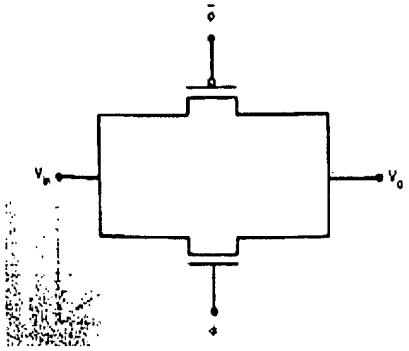

FIGURE 2.21. Transistor connection for CMOS transmission gate

- Complimentary switch (C-SWITCH) or Transmission gate
  - Pass a good 1 and a good 0.

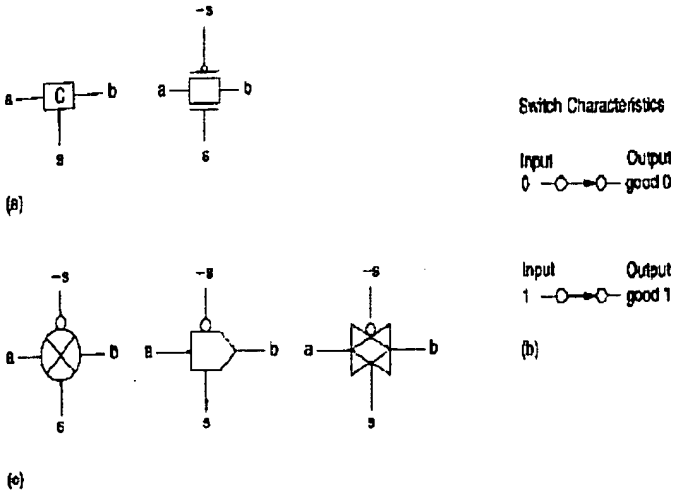

FIGURE 1.3 A complementary CMOS switch